WHAT IS CLAIMED IS:

1. A circuit designing apparatus comprising:

unit for specifying the changed points of the circuit description automatically in predetermined unit, and classifying the plural test vectors into those related with the changed points and others not.

2. A circuit designing apparatus comprising:

dividing unit for dividing a first circuit description defining the structure and specification of the circuit to be designed in predetermined units;

logic verification unit for verifying the logic by using said first circuit description and test vectors;

profile information generating unit for storing the information about the predetermined unit in the first circuit description to be activated by the test vector during said logic verification in every test vector as profile information;

circuit changing unit for changing said first circuit description and generating a second circuit description;

formal verification unit for verifying by formal technology using said first and second circuit descriptions;

specifying unit for specifying the changed predetermined unit relating to the change in said second circuit description on the basis of the result of said formal verification; and

test vector classifying unit for classifying the test vectors into those activating the changed predetermined unit and others not by using said profile information.

3. A circuit designing method comprising the steps of:

specifying the changed points of the circuit description automatically in predetermined unit; and

classifying the plural test vectors into those

related with the changed points and others not,

wherein the second and subsequent logic verification processes are executed by using only the test vectors relating to the changed points.

4. A circuit designing method comprising the steps of:

entering a first circuit description defining the structure and specification of the circuit to be designed;

dividing said first circuit description in predetermined units;

verifying the logic by using said first circuit description and test vectors;

storing the information about the predetermined unit in said first circuit description to be activated by the test vector during logic verification in every test vector as profile information;

changing said first circuit description and generating a second circuit description;

verifying by formal technology using the first and second circuit descriptions;

specifying the changed predetermined unit relating to the change in said second circuit description on the basis of the result of said formal verification; and

classifying the test vectors into those activating the changed predetermined unit and others not by using said profile information.

5. The circuit designing method of claim 4, wherein the logic verification of the second circuit description is executed by using preferentially the test vector for activating the changed predetermined unit.

6. The circuit designing method of claim 4, further comprising the step of:

issuing a circuit description and processing circuit

manufacture by using said circuit description.

7. The circuit designing method of claim 5, further comprising the step of:

issuing a circuit description and processing circuit design and manufacture by using said circuit description.

8. A computer-readable recording medium storing a circuit designing program comprising and making the computer execute the processes of:

dividing process for dividing a first circuit description defining the structure and specification of the circuit to be designed in predetermined units;

logic verification process for verifying the logic by using the first circuit description and test vectors;

profile information generating process for storing the information about the predetermined unit in the first circuit description to be activated by the test vector during logic verification in every test vector as profile information;

circuit changing process for changing the first circuit description and generating a second circuit description, formal verification process for verifying by formal technology using the first and second circuit descriptions;

specifying process for specifying the changed predetermined unit relating to the change in the second circuit description on the basis of the result of formal verification; and

test vector classifying process for classifying the test vectors into those activating the changed predetermined unit and others not by using the profile information.

9. The computer-readable recording medium storing a circuit designing program of claim 8, wherein the logic

verification of the second circuit description is executed by using preferentially the test vector for activating the changed predetermined unit.

10. The computer-readable recording medium storing a circuit designing program of claim 8, comprising and making the computer execute the process of:

output process of a circuit description,

wherein circuit manufacture is processed by using said circuit description.

11. The computer-readable recording medium storing a circuit designing program of claim 9, further comprising and making the computer execute the process of:

output process of a circuit description,

wherein circuit manufacture is processed by using said circuit description.